



USPTO

[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide



THE ACM DIGITAL LIBRARY


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)
Terms used: logic cone equivalence fpga dsp

Found 11,807 of 209,709

Sort results by

[Save results to a Binder](#)Try an [Advanced Search](#)

Display results

[Search Tips](#)Try this search in [The ACM Guide](#)
☐ Open results in a new window

Results 21 - 40 of 200

Result page: [previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

Relevance scale ☐ ☐ ☐ ☐ ☐

## 21 [CAD for FPGAs: Multiplexer restructuring for FPGA implementation cost reduction](#)



Paul Metzgen, Dominic Nancekievill

June 2005 **Proceedings of the 42nd annual conference on Design automation DAC '05**

Publisher: ACM Press

Full text available: [pdf\(691.28 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents a novel synthesis algorithm that reduces the area needed for implementing multiplexers on an FPGA by an average of 18%. This is achieved by reducing the number of Lookup Tables (LUTs) needed to implement multiplexers. The algorithm relies on reimplementing 2:1 multiplexer trees using efficient 4:1 multiplexers. The key to the algorithm's performance lies in exploiting the observation that most multiplexers occur in busses. New optimizations are employed which pay a small cost ...

**Keywords:** FPGA, busses, logic optimization, multiplexers, recoding, restructuring, synthesis

## 22 [Generation of very large circuits to benchmark the partitioning of FPGA](#)



Joachim Pistorius, Edm e Legai, Michel Minoux

April 1999 **Proceedings of the 1999 international symposium on Physical design ISPD '99**

Publisher: ACM Press

Full text available: [pdf\(1.01 MB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

## 23 [Restructuring logic representations with easily detectable simple disjunctive decompositions](#)



H. Sawada, S. Yamashita, A. Nagoya

February 1998 **Proceedings of the conference on Design, automation and test in Europe DATE '98**

Publisher: IEEE Computer Society

Full text available: [pdf\(125.30 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)  
[Publisher Site](#)

Simple disjunctive decomposition is a special case of logic function decompositions, where variables are divided into two disjoint sets and there is only one newly introduced variable. This paper presents that many simple disjunctive decompositions can be found


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)


[Advanced Scholar Search](#)  
[Scholar Preferences](#)  
[Scholar Help](#)

**Scholar** All articles - **Recent articles** Results 1 - 10 of about 5,450 for **logic equivalence dsp fpga**.

#### All Results

[Y Tzou](#)
[R Petersen](#)
[B Hutchings](#)
[R Andraka](#)
[H Hsu](#)

**An Assessment of the Suitability of FPGA-Based Systems for use in Digital Signal Processing - all 5 versions »**

RJ Petersen, BL Hutchings - 5th International Workshop on Field-Programmable Logic and ..., 1995 - splish.ee.byu.edu

... For comparison to **equivalent** implementations using 1-2 FPGAs ... for two custom FIR filter ASICs, the **Logic Devices** ... not unreasonable for a **FPGA-based DSP** system. This ...

Cited by 49 - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

**FPGA realization of space-vector PWM control IC for three-phase PWM inverters - all 4 versions »**

YY Tzou, HJ Hsu - Power Electronics, IEEE Transactions on, 1997 - ieeexplore.ieee.org

... grouped together as a configurable **logic** block (CLB ... 3. Circuit configuration of the **DSP-controlled FPGA** ... 5. **Equivalent** PWM switching patterns generated from three ...

Cited by 53 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**FPGA implementation of FIR filters using pipelined bit-serial canonical signed digit multipliers**

S He, M Torkelson - Custom Integrated Circuits Conference, 1994., Proceedings of ..., 1994 - ieeexplore.ieee.org

... addition, outperforms some dedicated commercial **DSP** chips ... can produce a near **equivalent** performance ... in wordlength latency with maximum **logic** level **equivalent** ...

Cited by 22 - [Related Articles](#) - [Web Search](#)

**DIGIT-SERIAL DSP LIBRARY FOR OPTIMIZED FPGA CONFIGURATION - all 9 versions »**

H Lee, GE Sobelman - Time (ns) - doi.ieeecomputersociety.org

... **FPGA** design with design based on **logic** synthesis for ... path delay of digit-serial **DSP** libraries are ... that have smaller area than **equivalent** parallel arithmetic ...

Cited by 5 - [Related Articles](#) - [Web Search](#)

**Implementation of a real-time frequency-selective RF channelsimulator using a hybrid DSP-FPGA ... - all 4 versions »**

MA Wickert, J Papenfuss - Microwave Theory and Techniques, IEEE Transactions on, 2001 - ieeexplore.ieee.org

... an asymmetric FIR filter, while introducing the **equivalent** group delay ... with a maximum of 80 000 **logic** gates. ... The **DSP** has enough available bandwidth to easily ...

Cited by 7 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**A flexible multiplication unit for an FPGA logic block - all 3 versions »**

K Rajagopalan, P Sutton - Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE ..., 2001 - ieeexplore.ieee.org

... including digital filters, correlators and other **DSP** applications ... architecture requires 3.6 times fewer **logic** blocks (2.8 times fewer **equivalent** gates) than ...

Cited by 7 - [Related Articles](#) - [Web Search](#)

**Programmable logic device for real time video processing - all 3 versions »**

B Taylor - US Patent 5,857,109, 1999 - Google Patents


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide

technology mapping load clear


**THE ACM DIGITAL LIBRARY**

[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

 Terms used: technology mapping load clear

Found 77,112 of 209,709

Sort results by

relevance


[Save results to a Binder](#)
[Try an Advanced Search](#)
[Try this search in The ACM Guide](#)

Display results

expanded form


[Search Tips](#)
☐ Open results in a new window

 Results 21 - 40 of 200    Result page: [previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

 Relevance scale ☐ ☐ ☐ ☐ ☐

## 21 [Level set and PDE methods for computer graphics](#)


 David Breén, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker  
 August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

 Full text available: [pdf\(17.07 MB\)](#)    Additional Information: [full citation](#), [abstract](#), [citations](#)

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

## 22 [Logic synthesis and mapping: Placement-driven technology mapping for LUT-based](#)


**FPGAs**

Joey Y. Lin, Ashok Jagannathan, Jason Cong

 February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

 Full text available: [pdf\(252.89 KB\)](#)    Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we study the problem of placement-driven technology mapping for table-lookup based FPGA architectures to optimize circuit performance. Early work on technology mapping for FPGAs such as Chortle-d[14] and Flowmap[3] aim to optimize the depth of the mapped solution without consideration of interconnect delay. Later works such as Flowmap-d[7], Bias-Clus[4] and EdgeMap consider interconnect delays during mapping, but do not take into consideration the effects of their mapping solution ...

**Keywords:** FPGA synthesis, logic re-synthesis, mapping

## 23 [Real-time shading](#)



Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi Rost

 August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

 Full text available: [pdf\(7.39 MB\)](#)    Additional Information: [full citation](#), [abstract](#)

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	altera.as. and loong	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:05
S2	1374	altera.as.	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:05
S3	8	altera.as. and (logic near3 cones)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:12
S4	20	altera and (logic near3 cones)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:49
S5	35	altera and (technology near3 map)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:56
S6	1	("6990650").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/08/26 14:15
S7	24	(technology near3 map) and fpga and dsp	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 14:16
S8	5	(technology near3 map) and fpga and dsp and ((ip or dsp) near3 block)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 14:16